ADVANCE INFO

7220
BUBBLE MEMORY CONTROLLER

- Ideal for IM's Bubble Memories
- Standard 8080/8085/Multibus™ Interface
- Multiple Bubble Module Interface Capability
- Self-Contained Timing Generation
- DMA Handshake Capability
- Single or Multiple Page Blo Transfers
- HMOS Technology
- Standard 40-Pin Dual In-Lin

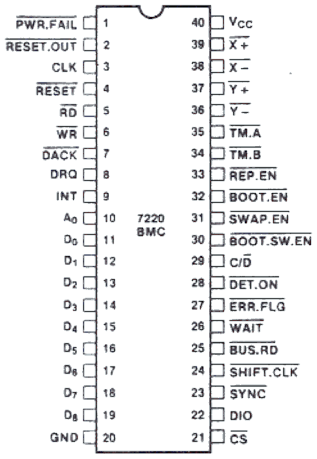
The Intel 7220 is a complete Bubble Memory Controller (BMC) designed to interface with Intel Ma Memories. The interface to the outside world is through the standard 8080/8085/Multibus™.

The 7220 is capable of multiple bubble memory interface. It has self-contained timing generation and I capability. Single and/or multiple page block transfers are also possible.

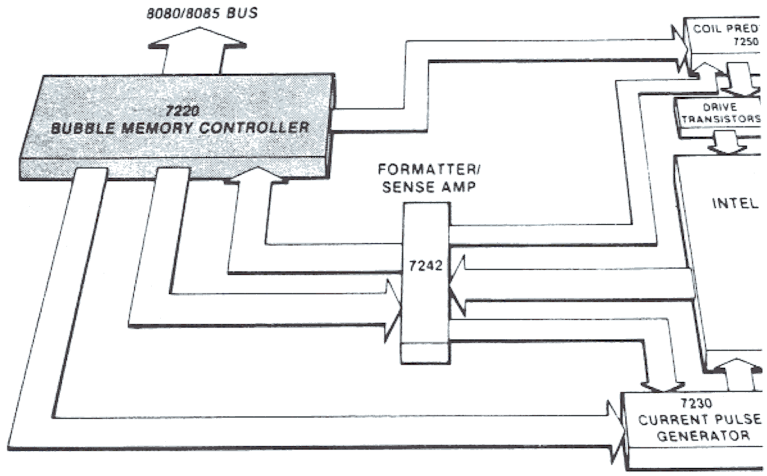
The 7220 is capable of interfacing with up to eight 7242 Dual Formatter/Sense Amplifier (FSA) devices. the bubble memory via the FSA is reformatted into a nine bit parallel bus (ninth bit is used for parity) interface.

The 7220 utilizes Intel's high performance HMOS technology. The device is packaged as a standard 4C package. All inputs and outputs are directly TTL compatible and the device uses a single +5 volt sup

PIN CONFIGURATION



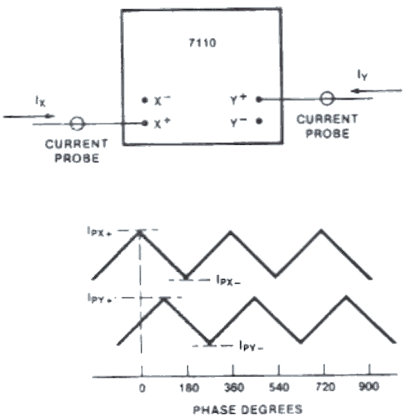
BLOCK DIAGRAM



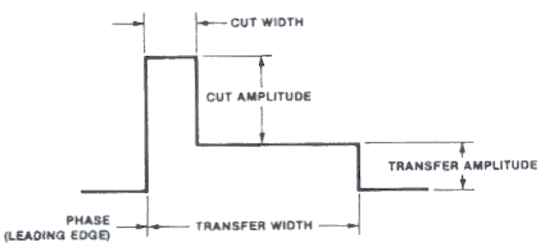
Block Diagram of Single Bubble Memory Syste

Table 1. 7110 Family

Part Number	T_A Range
7110	0–50°C
7110-1	0–70°C
7110-2	10–50°C
7110-3	10–35°C



3. Two level pulses are described as shown below.



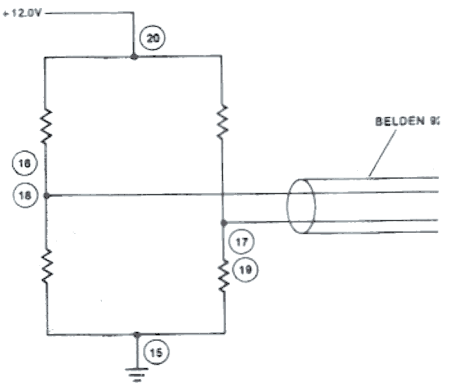
4. BOOT.SWAP is not normally accessed during operation. It is utilized at the factory to write the index address and redundant loop information into the bootstrap loops before shipment.

OUTPUT CHARACTERISTICS

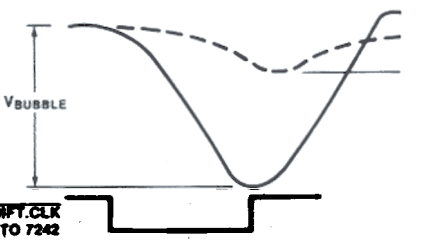
$T_A = 25°C$ unless otherwise specified.

	Min.	Nom.	Max.	Units
V_{BUBBLE}		8.0		mV
V_{NOISE}		1.5		mV

TEST SET-UP FOR OUTPUT VOLTA(MEASUREMENT



OUTPUT WAVEFORMS



PIN DESCRIPTION

A_0 (Pin 10)

An address pin used to select one of two internal registers. A logic "0" on this pin shall select the data register and a logic "1" shall select the command/status register.

$\overline{BOOT.EN}$ (Pin 32)

An active low signal enabling the bootstrap loop replicate function in external circuitry.

$\overline{BOOT.SW.EN}$ (Pin 30)

An active low signal which may be used for enabling the BOOT.SWAP of the 7230 CPG.

$\overline{BUS.RD}$ (Pin 25)

An active low signal that indicates that the DIO line is in the input mode. It shall be used to allow off-board expansion of 7242 FSA devices.

C/$\overline{D}$ (Pin 29)

A high on this line shall indicate that the BMC is beginning an FSA command sequence.

CLK (Pin 3)

The clock shall be a 2 to 5 MHz, 50% ± 10% duty cycle TTL clock.

$\overline{CS}$ (Pin 21)

Chip Select Input. A high on this pin shall disable the device to all but DMA transfers (i.e., it ignores bus activity and goes into a high impedance state).

$\overline{DACK}$ (Pin 7)

DMA acknowledge notifies the BMC that the next memory cycle is available to transfer data. This line should be active only when DMA transfer is desired and the DMA ENABLE bit has been set. $\overline{CS}$ need not be active during DMA transfers.

$\overline{DET.ON}$ (Pin 28)

An active low signal indicating that the magnetic bubble is detecting. It is useful for power saving in the MBM.

DIO (Pin 22)

A bidirectional, active high data line that shall be used for serial communications with 7242 FSA devices.

DRQ (Pin 8)

A logic high shall indicate that a transfer of data between BMC and host memory is being requested.

D_0-D_8 (Pins 11 through 19)

A nine bit bidirectional port which can be read or written by utilizing the RD and WR strobes. D_0 shall be the LSB. D_8 shall be a parity signal. When a byte is transferred to the BMC (over D_0-D_7), odd parity shall be generated by the BMC and compared to D_8. When a byte is transferred from the BMC to the host, odd parity over D_0-D_7 shall be generated and transferred as D_8. Errors in parity shall create an interrupt when enabled by the host CPU.

$\overline{ERR.FLG}$ (Pin 27)

An active low input generated externally by 7242 FSA indicating that an error condition exists.

INT (Pin 9)

A logic one shall indicate that the BMC has a new status and requires servicing when enabled by the host CPU.

$\overline{PWR.FAIL}$ (Pin 1)

A logic zero shall indicate that power has force the BMC to begin a controlled stop hold it in an idle state as RESET does.

$\overline{RD}$ (Pin 5)

Enables BMC to output data to the data l

$\overline{REP.EN}$ (Pin 33)

An active low signal used to enable the r tion in external circuitry.

$\overline{RESET}$ (Pin 4)

A logic zero on this pin forces the inter BMC sequencer activity, performs a cc down and initiates a RESET sequence. Af sequence is concluded a logic zero on thi logic zero on the $\overline{RESET.OUT}$ pin. Al sequence has been run the next BM commands must be either the initialize purge command. All other commands are

$\overline{RESET.OUT}$ (Pin 2)

An active low signal that disables externa be initiated by a $\overline{PWR.FAIL}$ or $\overline{RESET}$ sig not become active until the stopping p rotation is reached (if the BMC is causi memory drive field to be rotated).

$\overline{SHIFT.CLK}$ (Pin 24)

A controller generated clock that initiates between selected FSA's and their corresp memory devices. The timing on $\overline{SHIFT.C}$ depending upon whether data is being rea the bubble memory.

$\overline{SWAP.EN}$ (Pin 31)

An active low signal used to create the sv external circuits.

$\overline{SYNC}$ (Pin 23)

An active low output utilized to create multiplexing slots in a 7242 FSA chair indicate the beginning of a data or com between BMC and 7242 FSA.

$\overline{TM.A}$ (Pin 35)

An active low timing signal generated b logic for determining CUT pulse width.

$\overline{TM.B}$ (Pin 34)

An active low timing signal generated b logic for determining TRANSFER pulse v

$\overline{WAIT}$ (Pin 26)

A bidirectional pin that shall be tied to th other BMC's when operated in parallel. I that an error has been detected and th should halt until the type of error has be An active low signal.

$\overline{WR}$ (Pin 6)

Enables BMC to receive data from the d

$\overline{X+,X-,Y+,Y-}$ (Pins 39, 38, 37 and 36)

Four active low timing signals gen decoding logic and used to create coil d the bubble memory device.

FUNCTIONAL DESCRIPTION

Each block of the 7220 BMC is briefly described as follows:

System Bus Interface — The System Bus Interface (SBI) logic contains the timing and control logic required to interface the BMC to a non-multiplexed bus. The logic also contains the circuitry to check and generate parity (odd) on transfers across the bus. The interface has input data, output data, and status data latches.

FIFO — The FIFO is a 40 × 8 bit FIFO RAM for data storage. The FIFO RAM is dual port so that data may be read (written) at one port while simultaneously being written (read) at the other. It will be the responsibility of the host to make sure there is data/room available in the FIFO for transfers to/from the FSA's. If the host fails to keep up a timing error will result. The FIFO block also contains input and output data latches, providing double data buffering, to improve the R/W cycle times seen at the SBI. The FIFO may be used as a general purpose FIFO when a command is not being executed by the BMC Sequencer. In this mode, the FIFO READY status bit will become a FIFO absolutely empty indicator, which indicates that the RAM and input/output latches are all void of data.

DMA and Interrupt Logic — The BMC DRQ pin has two functions:

(1) If the DMA enable bit in the enable register is set, the DRQ pin, in conjunction with the $\overline{\text{DACK}}$ pin, provides a standard DMA transfer capability, i.e., it has the ability to handshake with an 8257 or 9517/8237 DMA controller chip.

(2) If the DMA enable bit is reset, the DRQ pin acts as a "ready for data transfer interrupt" pin. It becomes active when 20 bytes may be read from/written into the BMC, it is reset when this condition no longer exists.

This interrupt mode offers an alternative to polling the status word in medium performance systems when DMA is not used.

DI/O-Bootloop Decoder/Encoder — This block of circuitry does parallel to serial and serial to parallel conversion of data to generate the bidirectional DIO pin, which is the data bus line to FSA's in the Bubble system. It also generates the $\overline{\text{BUS.RD}}$ pin which identifies the direction of DIO data transfer if external buffering is required for the DIO line. This block also contains hardware to generate and decode the Bubble Bootstrap loop code during Read and Write Bootloop operations.

Sequencer — The BMC contains a microsequencer for control. The sequencer, by decoding the contents of the ROM, interprets commands, sets and resets flags and status bits, and initiates and terminates actions in other parts of the BMC.

MBM Address Logic and RAM — The logic consists of the block length co present address counter, an adder and tl RAM. The MBM address RAM is used t available page address for each half FSA's. The address maintained is the re write address is generated when need constant to the stored read address.

The block length counter enables transfers of up to 2048 pages in length

The start/present address counter is us to hold the desired start address. Once t is reached the counter is increme subsequent page transfer so that its v the present read address.

Register File — The register file cont registers that are accessible by the hos the Register Section for details.

Bubble Signal Decoder — The bubble logic contains the logic for creating timings. The logic consists of a three decoder, and synchronous latches.

The first stage is a modulo four counter or disabled by the host CPU via the "LC the enable register (see Register Sectic

The second stage is a modulo twenty create 40 clock edges within a field rot to this stage can be either the modulo the input clock.

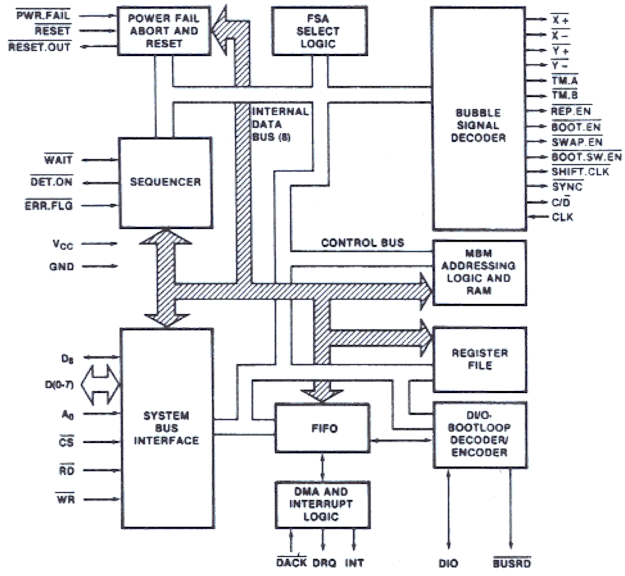
The third stage of the counter is a 12 bi input is the output of the second stag stage is used to count MBM field rotatio operations.

The outputs of both the second and thir are decoded to generate the set and rese MBM signal latches. Each MBM individually enabled by the sequencer, a reset on any edge of the second stage

FSA Select Logic — This logic determir contain the addressed data. Informat from the four upper order bits of th register and the four upper order bits register (see Register Section). The out is used by the DI/O-Bootloop Decc determine when valid data is availabl loaded, on the DIO line.

Powerfail, Abort and Reset — This logi a means of resetting the bubble syster manner. When activated by either the $\overline{\text{PF}}$ $\overline{\text{RESET}}$ pin, or a BMC abort commar forces a controlled shutdown of the bubble data integrity, and starts the se appropriate sequence.

LOGIC DIAGRAM

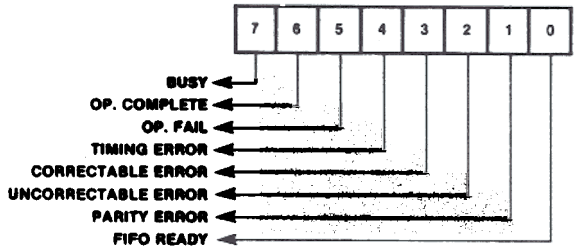


REGISTERS

Directly Addressable Registers — There are two registers in the BMC that are directly read or written from the data bus by the host CPU. They are the status/command register and the data register.

Status/Command Register — The status/command register is addressed by taking the address line A_0 to a logic one. When this register is read the BMC status is read (defined below). When this register is written the word is loaded in a dual purpose command register.

BMC Status:



BUSY — This bit indicates that the controller sequencer is still in the process of executing its last command. When the controller is ready to receive a new command the bit is set low.

OP COMPLETE — This bit is set upon successful completion of a command. It is reset whenever the status register is interrogated by the host.

OP FAIL — A logic one in this bit ind
BMC was unable to successfully comple
It is reset upon interrogation.

TIMING ERROR — This bit indicates th
reported a timing error, or the host has fa
with the BMC and the BMC FIFO has ove
empty. It is reset upon interrogation.

CORRECTABLE ERROR — Indicates th
reported a correctable error and shall be
terrogation.

UNCORRECTABLE ERROR — Indicates
data block transferred contained an uncc
It shall be reset upon interrogation.

PARITY ERROR — Indicates a parity ch
shall be reset upon interrogation.

FIFO READY — This bit indicates tha
available to be written or has data ready t
the busy bit is active. It indicates that
FIFO input and output registers are a
BUSY is inactive

Command Register — The command re
dual purpose. If Bit 4 is a logical 1, B
loaded as a BMC sequencer commanc
logical 0, then Bits 0-3 will be loaded ir
register counter (ARC), which is interpre

BMC Sequencer Commands:

NO OPERATION
INITIALIZE
READ
WRITE
READ SEEK
READ BOOTLOOP REGISTER
WRITE BOOTLOOP REGISTER
WRITE BOOTLOOP
READ FSA STATUS
ABORT
RESERVED
READ BOOTLOOP
READ CORRECTED DATA
FIFO RESET
MBM PURGE
SOFTWARE RESET

Address Register Counter (ARC):

RESERVED
"
"
"
"
"
"
R/W { COMMAND REG.
UTILITY REG.
BLOCK LENGTH LSB
BLOCK LENGTH MSB
ENABLE
ADDRESS LSB
ADDRESS MSB
FIFO

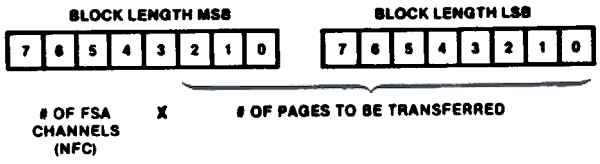
REGISTERS (continued)

DATA REGISTER — The source or destination of data read or written to the data register is specified by the register address counter (RAC). The RAC is set by writing to the status/command with Bit 4 a logical 0 and Bits 0-3 set to the corresponding desired register. Data may then be transferred by addressing the data register. Upon the completion of each data transfer the RAC is incremented to address the next register. After the RAC rolls over to zero, the FIFO address, all subsequent data transfers will sequentially access FIFO locations. The use of the RAC allows access to all registers with only one status/command operation.

FIFO Register — Data read or written into the FIFO is valid only when the FIFO READY bit is true in the status/command register.

Utility Register — The utility register is an 8 bit general purpose register.

Block Length Register — The block length registers are two eight-bit registers whose bits shall be interpreted as follows:

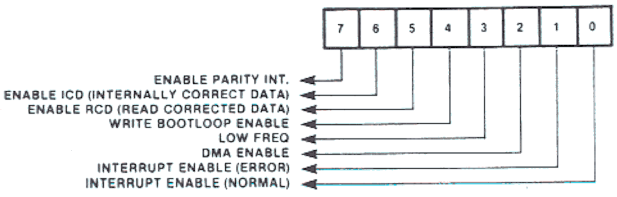


Since the BMC can interface with from one to sixteen channels of information, the four MSB's of the block length MSB register are used to specify the number of FSA channels (NFC) to be used in each transfer. The four MSB's shall be interpreted as follows:

	7	6	5	4
One FSA	0	0	0	0
Two FSA's	0	0	0	1
Four FSA's	0	0	1	1
Eight FSA's	0	1	1	1
Sixteen FSA's	1	1	1	1

These four bits, in conjunction with the address bits, determine which memory modules are being accessed for a given transfer.

Enable Register — The enable register contains flags set by the host that will enable or disable various functions within the BMC or FSA. The bits in the register are interpreted as follows:



Interrupt Enable (Normal) — A logic one shall enable the BMC to interrupt the CPU with the INT pin upon completion of a task.

Interrupt Enable (Error) — See Error Interr

DMA Enable — A logic one shall cause request data transfers via DRQ and $\overline{DA}$ logic zero shall cause all transfers to occ the status register or using DRQ as an Refer to functional description for DMA Logic.

Low Freq — This bit shall be set to enabl the divide by four counter in the timing the bubble memory timings are affect timing is unaffected. For 7110 set to on MHz clock.

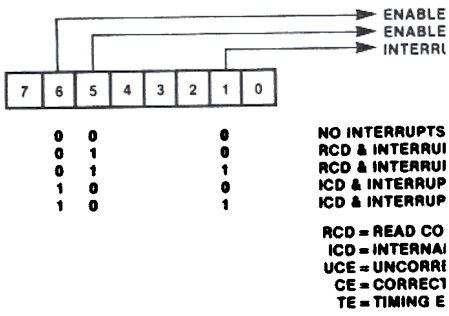
Write Bootloop Enable — This bit must b one if the bootstrap loop is to be rewritter and this command is received, it will be timing error will result.

Enable RCD — Enables the BMC to atte the data as it is passed to the BMC. In t uncorrectable error bad data may be pass

Enable ICD — Enables the BMC to attemp data errors before transferring the data error into host memory.

Enable Parity Interrupt — Enables the BM the host CPU upon detection of a parity er bus.

Error Interrupts — The status of interrup enable RCD, and enable ICD are decode the various error conditions under whicl interrupt the host CPU.



Address Registers — The address regis two eight bit registers whose bits are follows:

The eleven LSB's designate the starting the data transfer, regardless of the nun modules being accessed. The four MS the four MSB's of the block length reg which modules are to be accessed. Tab the FSA's that are to be used with variou of address and block length MSB's.

Table 1. FSA Channels Selected vs Address Bits

Block Length MSB	0000	0001	0011	0111
Address MSB				
0 0 0 0	0	0, 1	0, 1, 2, 3	0 to 7
0 0 0 1	1	2, 3	4, 5, 6, 7	8 to 15
0 0 1 0	2	4. 5	8, 9, 10, 11	—
0 0 1 1	3	6, 7	12, 13, 14, 15	—
0 1 0 0	4	8, 9	—	—
0 1 0 1	5	10, 11	—	—
0 1 1 0	6	12, 13	—	—
0 1 1 1	7	14, 15	—	—
1 0 0 0	8	—	—	
1 0 0 1	9	—	—	
1 0 1 0	10	—	—	—
1 0 1 1	11	—	—	—
1 1 0 0	12	—	—	—
1 1 0 1	13	—	—	—
1 1 1 0	14	—	—	—
1 1 1 1	15	—	—	—

COMMANDS

When a command is sent the BMC will be busy executing that command until 1) it is completed, 2) a fatal error occurs, 3) an ABORT command is sent, or 4) a power fail or hardware reset is executed. The commands are briefly described as follows:

No-Operation — Causes the BMC to enter an idle state.

Initialize — The initialize command starts by interrogating the bubble system to determine how many FSA's are present. The BMC then reads and decodes the contents of the bootstrap loop of each bubble device and stores the contents in the associated FSA bootstrap loop register. For dual FSA selection the (NFC) bits should be set to (0001). This allows the BMC to read both bootloops of the bubble and logically OR them together to create a bootloop redundancy factor. When the sequence is completed the BMC leaves each bubble module at a known address location and sets all BMC MBM address RAM locations to zero.

Read — Causes data to be transferred from bubble memory to BMC FIFO. Data is transferred from each bubble device selected per Table 1.

Write — Causes data to be transferred from BMC FIFO to bubble memory. Again, data is transferred to each bubble device per Table 1.

Seek — Causes the BMC to rotate the selected bubble device to the address specified and stop (no data transfers occur). The BMC stops the devices in such a manner that the next block available for a read is the specified address plus one.

Read Bootloop Register — Causes the BMC to read the contents of the selected FSA's bootloop register and store in FIFO. The data shall then be available to the host CPU. If more than one FSA is selected, bootloop register data will be interleaved.

Write Bootloop Register — Causes the BMC FIFO to be written into the selecte register. Twenty bytes are needed for ea since only 160 bits are required per FS/ than one FSA is selected, the host mus data properly.

Write Bootloop — Enables the host CPI existing contents of a bubble device boc stored in the BMC FIFO. Encoding is dc so only 40 bytes of data are required. A this command shall also require an enal the enable register.

Read FSA Status — Causes the BMC to status of all FSA's and store in the BMC I the entire status of all FSA's can be rea the first 16 bytes of the BMC FIFO with The host CPU shall then have access to

Abort — Intercepts the present BMC ac forms a controlled MBM shut-down to m integrity.

Read Bootloop — Causes the BMC to rea bubble device bootstrap loop, decode, results in the FIFO.

Read Corrected Data — Commands Form corrected data which is in FSA's FIFO.

FIFO Reset — Clears the BMC FIFO, a input/output latches.

MBM Purge — Clears all BMC registers, the MBM RAM except for the block lengt NFC, the FSA present counter, and the u of the start/present address counter. This be used if the host chooses to store the bo external PROM.

Software Reset — Resets all registers a except initialization parameters.

INTERFACES

CPU Interface — The BMC can interface asynchronously to the host CPU. With a 5 MHz clock, it is capable of sustaining a 1.6 Mbyte/sec transfer rate, while data/room is available in the BMC FIFO.

Software Interface — The general procedure for communicating with the BMC is:

(1) Read the status/command register until BMC is not busy.

(2) Pass parameters to the BMC by addressing the proper register.

(3) Examine the status register to determine whether the operation was successful.

Commands, status, and parameters sha
I/O commands. Data can be passed eit
mands or via a DMA channel.

Serial Interface — Refer to 7242 FSA Sp
description of the BMC/FSA interface.

Bubble Interface — The BMC/bubble m
consists of 10 active low timing signa
and stopping point of each signal is de
decoder logic. Each signal may occur
tion or only once in a number of field ro
rotation in which a timing pulse occurs
the sequence logic. Figure 1 illustrate
signals.

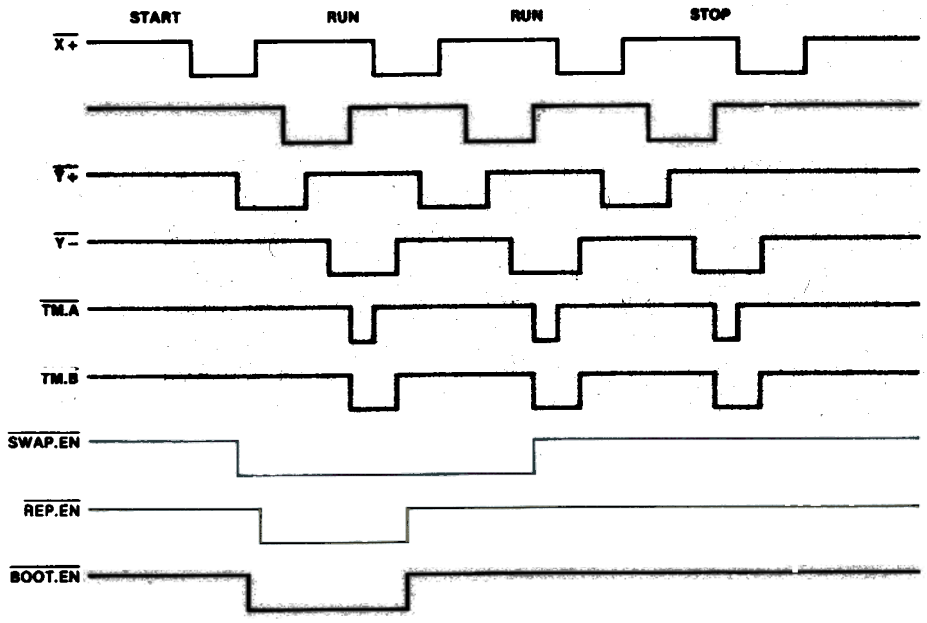


Figure 1. Typical Bubble Timing Signals